FOUNDATION FOR QUANTUM COMPUTING INNOVATION (FQCI)

DST-NQM T-Hub for Quantum Computing

Indian Institute of Science (IISc) Campus, Bengaluru – 560012, Karnataka, India

TENDER DOCUMENT: DOMESTIC REQUEST FOR PROPOSAL (RFP)

Two-Cover (Part-A: Technical & Qualification Bid; Part-B: Commercial Bid) Electronic / Sealed Tender

Tender Reference No: FQCI/NQM/QPU-CLOUD/2026-27/01

Item Description: Procurement of Cloud-Based Access to Quantum Processing Units (Superconducting, Quantum Annealing, and Neutral-Atom / Trapped-Ion Architectures) with Strict Acceptance Testing (SAT), Multi-Tenant Governance, and Enterprise Support SLAs for NQM Research Groups.

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SECTION 1: BID SCHEDULE & TENDER SUMMARY

#	Parameter	Details
1.1	**Tender Reference No.**	FQCI/NQM/QPU-CLOUD/2026-27/01
1.2	**Issuing Authority**	Foundation for Quantum Computing Innovation (FQCI), IISc Campus, Bengaluru
1.3	**Mode of Tendering**	Two-Cover System: Part-A (Technical & Eligibility Bid) and Part-B (Commercial Bid)
1.4	**Scope of Procurement**	Cloud-based QPU Compute Access, SDK Integration, Simulator Compute, Dedicated Support, and Administrative Governance across Lots A, B, and C
1.5	**Tender Release Date**	01 September, 2026
1.6	**Pre-Bid Clarification Meeting**	07 September, 2026, at 15:00 IST (Online Mode: MS Teams Secure Video Link)
1.7	**Last Date for Submission of Bids**	30 September, 2026, up to 15:00 IST
1.8	**Opening of Part-A (Technical Bids)**	01 October, 2026, at 11:00 IST
1.9	**Opening of Part-B (Commercial Bids)**	To be communicated to technically qualified bidders following evaluation
1.10	**Bid Validity**	Minimum 30 days from the date of commercial bid opening
1.11	**Contract Duration**	Initial period of one (1) year, extendable on a yearly/quarterly basis up to an additional two (2) years (Total 3 Years) subject to satisfactory SAT compliance and SLA performance
1.12	**Address for Communication & Submission**	Chief Operating Officer, Foundation for Quantum Computing Innovation (FQCI), C/o Indian Institute of Science (IISc), Bengaluru – 560012, Karnataka, India. E-mail: info@qcinnovation.co.in ; venkatps@qcinnovation.co.in

SECTION 2: BIDDER ELIGIBILITY & PRE-QUALIFICATION CRITERIA

Bidders must fulfil the following mandatory pre-qualification criteria. Failure to satisfy any criterion will result in summary rejection of the bid during Stage-1 evaluation.

#	Mandatory Eligibility Criterion	Requirement
1	**Indian Entity Presence**	Mandatory registered Indian subsidiary, HQ, or office.
2	**Financial Stability**	Positive net worth; audited financial statements for the last 3 years.
3	**Experience & Deployments**	Established production deployments in research/academia.
4	**Clean Track Record**	No debarment or blacklisting in India or abroad.
5	**IP & Data Security / Non-Leakage**	Zero training on client circuits; strict compliance with IP and data security requirements.

1. **Indian Entity & Corporate Presence:**
    - The Bidder must be an Original Quantum Equipment Manufacturer (OEM) or an authorized cloud service distributor/subsidiary having a **registered office, sales, and dedicated technical support operations in India** incorporated under the Companies Act, 2013.
    - The Indian entity must be authorized to enter into legally binding contracts, issue GST-compliant invoices in Indian Rupees (INR), and provide Tier-1/Tier-2/Tier-3 technical support during Indian Standard Time (IST) business hours.
2. **Financial Standing:**
    - The Bidder (or its parent OEM) must demonstrate financial viability with audited balance sheets and profit & loss statements for the last three financial years (FY 2023–24, 2024–25, and 2025–26) certified by a Chartered Accountant / Certified Public Accountant.
    - The Bidder must have a positive net worth in each of the last three financial years.
3. **Operational Track Record:**
    - The Bidder/OEM must have provided cloud-based QPU access or quantum computing services to at least three (3) recognized academic institutions, national laboratories, or Fortune 500 R&D centres in India or globally within the last three (3) years. Supporting purchase orders (with masked prices if necessary), service agreements, Client Letters/Certificates, or a Self-Declaration/Affidavit from the bidder must be submitted, as applicable.
4. **Clean Track Record & Non-Blacklisting:**
    - The Bidder must not have been banned, debarred, suspended, or blacklisted by any Central/State Government Ministry, Department, Public Sector Undertaking

(PSU), Autonomous Institute, or international regulatory agency. A self-declaration on official letterhead must be submitted (**Annexure 3**).

5. **Tax & Legal Registrations:**
    - The Bidder must possess a valid Permanent Account Number (PAN), Goods and Services Tax (GST) registration in India, and an up-to-date GST return filing clearance.

SECTION 3: INSTRUCTIONS TO BIDDERS & EVALUATION FRAMEWORK

3.1 Two-Cover Submission Protocol

The tender must be submitted in two separate sealed covers (or two password-protected cryptographic electronic archives if e-tendering):

Bid Component	Documents / Information to be Submitted	Key Requirement
Envelope A: Technical Bid	Annexures 1 through 7	Technical documentation
	Compliance Statement (5 Columns)	Mandatory
	Audited Financial Statements	Mandatory
	OEM Authorization & SAT Undertaking	Mandatory
	Pricing Information	**Strictly prohibited**
Envelope B: Commercial Bid	Lot-wise Rate Cards (INR)	Mandatory
	Dedicated & Shared Hourly Rates	Mandatory
	Shot & Task Fees	Mandatory
	Total Cost of Ownership (TCO)	Mandatory
	Price Validity	**Prices firm for 3 years (INR)**

1. **Cover "A" (Technical Bid):** Shall contain all technical specifications, vendor declarations, administrative portal details, SAT execution plans, and Annexures 1 through 7. No pricing or commercial information shall be included in Cover "A". Any breach will result in immediate disqualification.
2. **Cover "B" (Commercial Bid):** Shall contain the Lot-wise pricing schedules (Shared Queue rates, Dedicated Reservation rates, Per-Task fees, and Per-Shot fees) strictly adhering to **Annexure 8** in Indian Rupees (INR).

3.2 Evaluation Methodology (Quality-Based Technical Qualification & Lowest Cost L1)

Evaluation will follow a three-stage process. **Technical and commercial offers will be evaluated separately and independently for each Lot.** Bidding on multiple Lots will neither penalize nor confer an unearned advantage in the individual scoring of any single Lot.

[STAGE 1: BID SUBMISSION]

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[Mandatory Eligibility Gate (Pass/Fail)]

├— Indian Legal Entity & Support Desk

├— Financial Standing & Track Record

└── Technical Specification Compliance

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(PASS ONLY)

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[STAGE 2: TECHNICAL SCORING]

├── Technology Breadth & Integration

├── Advanced Features (QML/AI/Var)

└── Support, Training & Ecosystem

↓

(QUALIFIED)

↓

[STAGE 3: COMMERCIAL EVALUATION]

└── Cost Efficiency & Pricing (INR)

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[FINAL CONTRACT AWARD]

Stage 1: Mandatory Compliance & Pre-Award Acceptance Test

- **Compliance Gate:** Bids are initially scrutinized for adherence to legal presence, financial stability, IP protection, and minimum RFP specifications.
- **Pre-Award Acceptance Test:** FQCI may choose to execute an active technical acceptance test on the vendor's proposed hardware to physically validate claimed metrics (e.g., fidelities, coherence, and baseline execution suitability) prior to technical qualification, particularly for unestablished providers. If FQCI opts to conduct this test, bidders failing the validation will be summarily rejected.

Stage 2: Technical Scoring (100 Marks per Lot)

Bidders passing Stage 1 will be evaluated against the technical rubric below. A bidder must score a minimum of 75 out of 100 marks to qualify for commercial opening.

#	Evaluation Category	Sub-Criteria & Scoring Focus	Maximum Marks
1.0	**Technology Breadth & Integration**		**50 Marks**
1.1	Qubit Fidelity & Physical Capacity	Verification of physical qubit count, single/two-qubit gate fidelities, readout fidelities, and coherence times (T_1/T_2) exceeding minimum RFP baselines.	25 Marks

1.2	SDK Integration & OpenQASM 3.0	Ssupport and compiler integration for Qiskit, PennyLane, Cirq, CUDA-Q, and OpenQASM 3.0 intermediate representation.	10 Marks
1.3	Calibration Telemetry & Pulse Control	Real-time programmatic API access to daily drift logs, cross-talk matrices, and pulse-level control capabilities.	10 Marks
1.4	Scientific Impact & Published Literature (5 Marks)	Evaluation of the top 5 to 10 submitted peer-reviewed publications demonstrating the practical viability and scientific utility of the specific QPU hardware offered through the vendor's service.	5 Marks
2.0	**Advanced Compute Features (QML / AI / Algorithms)**		**30 Marks**
2.1	Algorithmic Suitability (QML / VQE / QAOA)	Hardware efficiency for variational algorithms, hybrid quantum-classical loops, and quantum machine learning workloads.	15 Marks
2.2	Error Mitigation & Simulation Toolchain	Availability of software mitigation (ZNE, Dynamical Decoupling) or Analog Rydberg Hamiltonian simulation (Lot C) / QUBO scaling (Lot B)/ Support through the platform or integrated toolkits	15 Marks
3.0	**Support, Training & Ecosystem**		**20 Marks**
3.1	Support SLA Commitments	Adherence to L1/L2/L3 support tier definitions and resolution timelines (P1 $<$ 4h, P2 $<$ 12h, P3 $<$ 2d).	10 Marks
3.2	Capacity Building & User Training	Annual advanced workshops, documentation depth, and structured onboarding curriculum for the 106 researchers across 45 institutes.	10 Marks
TOTAL	**TECHNICAL QUALIFICATION SCORE**	***(Minimum Qualification Cutoff: 75 / 100 Marks)***	**100 Marks**

Stage 3: Commercial Evaluation (Lowest Cost / L1)

- Commercial bids (Cover "B") will be opened only for vendors who achieve the minimum technical cutoff of 75 marks in Stage 2.
- The contract for each respective Lot will be awarded to the technically qualified bidder submitting the lowest total commercial cost (L1) for that specific Lot.
- Commercial criteria such as price validity (3 years) and unconditional quarterly rollover of unused hours remain mandatory compliance requirements.

SECTION 4: GENERAL TERMS & CONDITIONS OF CONTRACT (GCC)

4.1 Contract Term, Extensions, and Milestone Reviews

1. The initial contract shall be executed for **one (1) year**.
2. The contract is extendable for **two (2) additional years** (one year at a time, up to a total of 3 years) subject to quarterly performance reviews, Strict Acceptance Testing (SAT) verification, and SLA adherence.
3. Performance will be audited at the end of each operating quarter. If the vendor fails to maintain hardware uptime, calibration fidelities, or resolution timelines, FQCI reserves the right to terminate the contract with a 30-day notice without financial liability.

4.2 Price Firmness, Rollover, and Foreign Exchange Adjustments

1. **Firm INR Pricing:** All rates quoted in the commercial bid must remain **fixed and firm for the entire three (3) year duration**.
2. **Rollover of Unused Compute:** Any unutilized quantum compute hours, dedicated slot reservations, or execution credits allocated in a given month/quarter shall **automatically roll over** to subsequent quarters/years across the contract lifecycle/ **automatically be converted** to credits for future QPU, simulator, or classical compute. Unused credits will not expire at the end of financial quarters.
3. **RBI Reference Mechanism:** Prices are billed in INR. Annual currency review mechanisms tied strictly to Reserve Bank of India (RBI) reference rates are permissible only if explicitly defined and capped in the commercial bid.

4.3 Intellectual Property (IP) Protection & Non-Disclosure

1. **Exclusive IP Ownership:** All quantum circuits, custom-developed variational algorithms, Hamiltonian models, hybrid workflows, pulse schedules, compiled binaries, raw job measurement outputs, and intermediate data generated by NQM researchers and participating institutions shall remain the **sole and exclusive intellectual property of the NQM, FQCI, and the respective researchers/institutions**.
2. **Prohibition of Data Reuse / AI Training:** The vendor, cloud hosting provider, and QPU backend OEM are strictly prohibited from inspecting, caching, reverse-engineering, harvesting, or utilizing any user data, circuit topologies, or execution traces for training classical machine learning models, optimizing internal proprietary algorithms, or any commercial purpose without prior written authorization.
3. **Execution of Non-Disclosure Agreement (NDA):** The successful bidder must execute a comprehensive Non-Disclosure Agreement (**Annexure 6**) prior to issuance of access credentials and deployment of tenant spaces.

4.4 Data Privacy, Localization, and Security Compliance

1. **Data in Transit & at Rest:** All API communications, administrative interactions, job submissions, and measurement telemetry must be encrypted in transit using **TLS 1.2 or higher** and at rest using **AES-256** encryption standards.

2. **Regulatory Compliance:** The vendor must ensure that identity registries, access management metadata, and telemetry pipelines strictly comply with Indian Data Protection Regulations and institutional security frameworks.

4.5 Payment Terms & Invoicing

1. **Quarterly Billing Cycle:** All payments for cloud QPU services shall be calculated and released on a quarterly basis at the end of each operational quarter.
2. **Payment Processing Timeline:** FQCI shall process and disburse the payment within two (2) weeks (14 business days) strictly following the receipt of a valid and complete invoice.
3. **Mandatory Supporting Documentation:** The clearance of any quarterly bill is strictly conditional. For an invoice to be considered complete and ready for processing, the vendor must submit the following alongside the bill:
    - **Detailed Monthly Usage Reports:** Comprehensive logs covering the respective quarter, detailing the exact compute hours, tasks, and shots consumed, broken down by the individual research institutes and the authorized users.
    - **Performance Evaluation Certificate:** A formal certificate of satisfactory performance (confirming successful SAT clearance and SLA adherence) issued by the FQCI Hub Technical Evaluation Committee for that specific quarter.

4.6 Capacity Provisioning & Expected Usage Estimates To enable vendors to accurately provision their backend systems and offer highly optimized pricing, FQCI provides the following estimated compute requirements:

1. **Approximate Monthly Volume:** Vendors should provision their systems to support an estimated **30 to 40 hours of QPU compute time per month** across all NQM user groups.
2. **Approximate Overall Volume:** The total expected QPU compute volume over the 3-year contract term is projected at **1400 hours**. *(Note: These figures are provided as baseline estimates for infrastructure provisioning and rate card calculation. Actual billing will be executed based on realized usage, reserved quotas, and strict adherence to the rollover mechanisms defined in Section 4.2).*

4.7 System Access & Admin Logins

- **Mandatory Master Logins:** The vendor must provision and maintain at least two (2) dedicated master administrative logins specifically for the FQCI Hub administration. These logins must provide overarching visibility into platform usage, quotas, and billing.
- **User & Institute Access:** This administrative access is strictly in addition to the standard user access that must be provisioned for the authorized researchers across the participating NQM institutes.

4.8 Scientific Publications & Validation

Bidders must provide a curated list of the top 10 peer-reviewed scientific publications that have been executed on and resulted directly from the specific quantum machines offered through their service platform. Exhaustive lists of hundreds of publications are discouraged. If the bidder acts as a cloud broker, the publications must correspond to the exact backend hardware models being proposed in the bid.

SECTION 5: DETAILED TECHNICAL SPECIFICATIONS

Bidders may bid for one, two, or all three Lots. Each Lot will be evaluated independently.

Parameter	Lot A – Superconducting QPUs	Lot B – Quantum Annealing & Analog Optimization	Lot C – Neutral-Atom & Trapped-Ion
Qubit Capacity	≥ 50 Physical Qubits	≥ 2,000 Active Qubits OR Analog ≥ 200 programmable atomic sites	≥ 50 Physical Qubits
1-Qubit Fidelity	≥ 99.9% (Median)	—	≥ 99.9% (Median)
2-Qubit Fidelity	≥ 99.0% (Median)	—	≥ 99.5% (Median)
Readout Fidelity	≥ 97.0% (Median)	—	≥ 98.5% (Median)
Coherence	T1>100 µs T2>60 µs	—	—
Quantum Volume / CLOPS	QV ≥ 128 **OR** CLOPS ≥ 5,000/ Vendor to declare QV and/or CLOPS	—	—
Graph Connectivity	—	Graph Degree ≥ 15 OR Programmable atom geometries with tunable interaction range	All-to-All / Reconfigurable
Problem Representation	—	QUBO / Ising Support	—
Performance Reporting	—	Time-to-Solution Reporting	—
Logical Variables	—	≥ 500 Logical Variables	—
Software / APIs	Data accessible via API	Python SDK & Embedding APIs	—
Simulation Capability	—	—	Analog Simulation Support

5.1 LOT A: Superconducting Quantum Computing Hardware (Gate-Based)

Stage / Component	Requirement / Specification
Input	Gate-Based Circuit
Compilation	Pulse / Compiler
QPU	Superconducting QPU
Coherence	T1>100 µs T2>60 µs
1-Qubit Gate Fidelity	≥ 99.9% (Median)
2-Qubit Gate Fidelity	≥ 99.0% (Median)
Readout Fidelity	≥ 97.0% (Median)

- **Physical Qubits:** ≥ 50 physical, actively calibrated superconducting qubits for primary production systems.
- **Single-Qubit Gate Fidelity:** $\geq 99.9\%$ (Median across operational lattice).
- **Two-Qubit Gate Fidelity:** $\geq 99.0\%$ (Median for 2-qubit entangling gates, e.g., CZ, ECR, CX, or iSWAP).
- **Readout Fidelity:** $\geq 97.0\%$ (Median across all active qubit readout channels).
- **Coherence Times:** $T_1 \geq 100\ \mu$s and $T_2 \geq 60\ \mu$s (Median across active qubits).
- **System-Level Benchmarks:** Quantum Volume (QV) ≥ 128 **OR** Circuit Layer Operations Per Second (CLOPS) $\geq 5{,}000$/ Vendor to declare QV and/or CLOPS.
- **Error Mitigation:** Software-level and compiler-level error mitigation tools (Zero Noise Extrapolation [ZNE], Probabilistic Error Cancellation [PEC], Dynamical Decoupling [DD], and Readout Twirling) / Support through the platform or integrated toolkits.
- **Telemetry & Calibration Access:** Real-time programmatic API access to daily calibration logs, drift histories, coherence times (T_1/T_2), cross-talk data where available, and device coupling maps.

5.2 LOT B: Quantum Annealing Hardware

Stage / Component	Requirement / Specification
Input	QUBO / Ising Problem
Embedding	Embedding & Minor Graph
Annealing Core	≥ 2,000 Qubits OR Analog ≥ 200 programmable atomic sites
Connectivity	Degree ≥ 15 OR Programmable atom geometries with tunable interaction range
Logical Variables	≥ 500

Performance Metrics	Time-to-Solution (TTS) / Residual Energy Logs

- **Active Physical Qubits:** $\geq 2{,}000$ active, interconnected physical qubits.
- **Hardware Topology:** High-degree connectivity topology graph with a minimum degree of 15 (e.g., Pegasus, Zephyr, or equivalent dense topologies).
- **Problem Formulation:** Support for Quadratic Unconstrained Binary Optimization (QUBO) and Ising spin-glass formulations with fully programmable linear biases (h_i) and pairwise coupling terms (J_{ij}) OR Programmable Hamiltonian for optimization.
- **Logical Variable Capacity:** Support for at least 500 fully connected logical variables for sparse and structured optimization problems.
- **Performance Reporting:** Automated reporting of Time-to-Solution (TTS), energy distribution histograms, residual energy, and scaling metrics per job execution.
- **API & Toolchain:** Full Python SDK integration OR Analog Python SDK with atom layout and Hamiltonian construction with automated minor-embedding algorithms, reverse annealing, and pause/quench schedule capabilities.

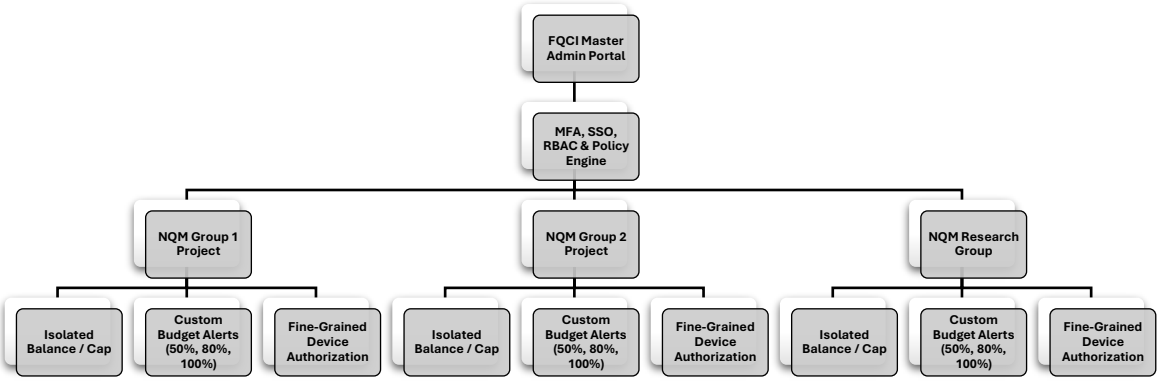
5.3 LOT C: Neutral-Atom and Trapped-Ion Hardware (Gate-Based & Analog)

Parameter	Trapped-Ion System	Neutral-Atom System
Connectivity	All-to-All Full Connectivity	Dynamically Reconfigurable
Single-Qubit Fidelity	≥ 99.9% (Median)	—
Two-Qubit Fidelity	≥ 99.5% (Median)	—
Readout Fidelity	≥ 98.5% (Median)	—
Simulation Capability	—	Programmable Hamiltonian Analog Simulation Modes
Physical Architecture	—	Optical Tweezer Geometry Array

- **Physical Qubits / Atom Capacity:** ≥ 50 physical qubits for gate-based processing or ≥ 100 atomic sites for analog simulation arrays.
- **Connectivity Architecture:**
    - *Trapped-Ion:* All-to-all qubit connectivity.
    - *Neutral-Atom:* Dynamically reconfigurable 2D/3D optical tweezer arrays with field-programmable geometric arrangements.
- **Gate Fidelities (Gate-Based Mode):**

    - Single-Qubit Gate Fidelity: $\geq 99.9\%$ (Median).
    - Two-Qubit Gate Fidelity: $\geq 99.5\%$ (Median).
    - Readout Fidelity: $\geq 98.5\%$ (Median).
- **Coherence Characteristics:** T_1 and T_2 coherence figures exceeding 100 μs operational benchmark equivalents (or second-scale coherence for atomic/hyperfine ground states).
- **Analog Simulation Capability:** Programmable Rydberg Hamiltonian simulation mode supporting quantum many-body dynamics, quantum spin liquids, and continuous-variable optimization.
- **Error Mitigation:** Support for dynamical decoupling, state preparation and measurement (SPAM) error mitigation, and zero noise extrapolation// Support through the platform or integrated toolkits.

SECTION 6: MULTI-TENANT GOVERNANCE, PLATFORM & SECURITY



1. **Centralized Administrative Portal:**
    - Unified administrative dashboard supporting a minimum of twenty (20) authorized institute managers and institutional Principal Investigators (PIs) with mandatory Multi-Factor Authentication (MFA) and Role-Based Access Control (RBAC).
2. **Multi-Tenant Governance for Research Groups:**
    - Complete account-level isolation and credential partitioning across the **distinct NQM research groups**.
    - Granular quota allocation engine enabling FQCI administrators to set hard/soft execution time limits, shot caps, and per-device spend ceilings per group.
    - Automated email notifications and webhooks triggered at **50%, 80%, and 100%** quota consumption thresholds.
3. **Usage Telemetry & Audit Reporting:**
    - Real-time accounting interface exporting JSON/CSV reports detailing execution timestamps, wait-in-queue durations, shot counts, circuit depth, gate counts, execution runtime, and billing charges broken down by user, project code, and QPU device.
4. **Open-Source SDK & Framework Interoperability:**
    - Out-of-the-box compilation and circuit submission support for at least three (3) of the primary quantum SDKs: **Qiskit, PennyLane, CUDA-Q, and Cirq**.
    - Compatibility with **OpenQASM 3.0** intermediate representation.
5. **Access Policy Enforcement:**
    - Policy engine enabling dynamic white-listing/black-listing of specific physical QPUs or high-demand systems on an institution-by-institution basis.

SECTION 7: STRICT ACCEPTANCE TESTING (SAT), SLAs, SUPPORT TIERS & PENALTIES

Step	Acceptance Test / Activity	Outcome / Action
Step 1	Automated Telemetry Ingestion — T1, T2, 1Q / 2Q / Readout Fidelities	Verify and record system performance metrics
Step 2	Synthetic Benchmark Execution — Quantum Volume / Randomized Benchmarking	Validate QPU performance against defined benchmarks
Step 3	72-Hour Continuous API Queue & Execution Stability Run	Verify sustained API, queue, and execution stability
Step 4	Governance Verification — Tenant Isolations, Quotas, Alerts	Validate multi-tenant governance and controls
SAT Passed	All acceptance criteria successfully met	**Quarterly Service Clearance & Payout Release**
SAT Failed	One or more acceptance criteria not met	**Immediate Remedy Window (14 Days) / Payment Holdback**

7.1 Strict Acceptance Testing (SAT) Protocol & Payout Linkage

No commercial disbursement, milestone advance, or quarterly payout will be authorized until the vendor successfully passes the **Strict Acceptance Testing (SAT)** administered by the FQCI Technical Evaluation Committee. SAT shall be executed:

- Solely for quarterly tracking and payment release during the 3-year term.

Mandatory SAT Verification Suite

1. **Automated Fidelity & Coherence Validation:**
    - Run automated Randomized Benchmarking (RB) and Readout Characterization across all operational qubits.
    - Median 1-qubit fidelity must meet or exceed 99.9%, median 2-qubit fidelity must meet or exceed 99.5%, and readout fidelity must meet or exceed 98.5%. Coherence times (T_1, T_2) must meet or exceed $100\ \mu$s.
2. **System Benchmark Execution:**
    - Gate-Based QPUs: Successful execution and verification of Quantum Volume ($QV \geq 128$) or validated throughput ($CLOPS \geq 5{,}000$).
    - Annealing Systems: Successful embedding and energy minimization of a 500-variable reference problem with verification of Time-to-Solution (TTS) scaling.
3. **Continuous 72-Hour Multi-Tenant Stability Test:**
    - Concurrent submission of automated test circuits across the isolated tenant accounts without API crashes, dropped jobs, or cross-tenant data leakage.

4. **Remedy Period:** If the system fails SAT, the vendor has **fourteen (14) calendar days** to rectify calibration, software, or configuration issues. Continued failure beyond 14 days entitles FQCI to cancel the quarterly allocation without payment obligation and invoke performance guarantees.

7.2 Support Tier Framework (L1, L2, L3)

The vendor must provide comprehensive Tier-1, Tier-2, and Tier-3 technical support embedded within the quoted rates without additional retainer fees:

Support Tier	**Scope & Technical Domain**	**Delivery Channel**
L1 Support *(Basic IT & Portal Access)*	Portal login authentication, MFA resets, credential management, quota balance checks, basic billing queries, and syntax/compiler error messages.	Cloud Helpdesk, Ticketing Portal & Email
L2 Support *(Quantum SDK & Software)*	API dropouts, SDK compilation errors, OpenQASM translation bugs, circuit transpilation failures, simulator mismatches, and pulse schedule anomalies.	Dedicated Quantum Application Engineers
L3 Support *(Hardware, Calibration & Physics)*	Physical QPU calibration failures, system timeouts, severe readout/gate error rate spikes, hardware decoherence degradation, and unannounced hardware downtime.	OEM Hardware Physicists & Senior Engineering Leads

7.3 Service Level Agreements (SLAs) & Incident Resolution Timelines

Severity Level	**Operational Impact**	**Response Time**	**Resolution Time**
P1: Critical Breakdown	QPU / API inaccessible	< 1 Hour	< 4 Hours
P2: Urgent Degradation	High errors / Queue stuck	< 4 Hours	< 12 Hours
P3: Standard Technical	SDK query / Transpiler flag	< 1 Day	< 2 Days
Severity Level	**Operational Definition**	**Mandatory Response Time**	**Target Resolution Time**
P1: Critical (System Down)	QPU platform or API endpoint completely inaccessible; jobs failing across all accounts; entire research pipeline blocked.	< 1 hour	< 4 hours *(or immediate automatic routing to backup identical simulator/hardware)*
P2: Urgent (Degraded State)	Jobs trapped in queue past maximum queue threshold; error rates significantly higher than published daily calibration	< 4 hours	< 12 hours

	standards; specific QPU nodes disabled.		
P3: Standard (Technical Query)	General inquiries regarding code compilation, compiler optimization flags, pulse scheduling APIs, or new SDK feature releases.	< 1 business day	< 2 business days

7.4 Quantum Uptime, Calibration Windows & Liquidated Damages

1. **Service Availability Targets:**
    - Cloud Management Interface, APIs, and Classical Simulators: $\geq 99.5\%$ **monthly uptime/ Vendor publishes scheduled availability 7 days ahead**.
    - Physical Quantum Processing Units (QPUs): $\geq 90.0\%$ **monthly uptime** (calculated after excluding pre-announced daily calibration windows) **/ Vendor publishes scheduled availability 7 days ahead**.
2. **Scheduled Calibration Windows:**
    - Daily or bi-daily cryostat/laser calibration routines must be scheduled during **off-peak hours relative to Indian Standard Time (IST)**.
    - Calibration windows must be announced at least 24 hours in advance and excluded from active job wait-time statistics.
3. **Maximum Single Breakdown Limit:**
    - Any continuous single hardware outage shall not exceed **twenty-four (24) hours**.
    - If an outage exceeds 24 hours, the vendor must automatically provision equivalent compute time on an identical or higher-tier QPU modality at no extra cost.
4. **Compensatory Service Credits (Liquidated Damages):**
    - If the vendor fails to meet the monthly availability targets or resolution timelines, the vendor must provide $1.5\times$ **compensatory service credit** for the entire compute duration lost during the outage:

$$\text{Compensatory Credit} = 1.5 \times (\text{Duration of Breakdown}) \times (\text{Committed Hourly Allocation Rate})$$

    - These credits shall be directly added to FQCI's remaining 3-year quota reserve without altering the contract price.
5. **Penalty for Unprovided Hours:** If the vendor fails to provide the total agreed-upon provisioned compute hours within the stipulated quarterly billing cycle, FQCI will impose a proportional financial penalty deducted directly from the quarterly invoice, in addition to the $1.5\times$ compensatory service credits for specific downtime incidents.

SECTION 8: ANNEXURES & SUBMISSION FORMATS

ANNEXURE 1: BIDDER PROFILE & CORPORATE DETAILS

(To be printed on Bidder's Official Letterhead, Signed & Stamped by Authorized Signatory)

To:

The Chief Operating Officer,

Foundation for Quantum Computing Innovation (FQCI),

IISc Campus, Bengaluru – 560012, Karnataka, India.

Ref: Tender Ref No. FQCI/NQM/QPU-CLOUD/2026-27/01

#	Parameter	Bidder Submission Details
1	Name of the Bidding Entity	
2	Nature of Legal Entity (OEM / 100% Subsidiary / Partner)	
3	Date & Country of Incorporation (Attach Certificate)	
4	Registered Address of Indian Office / Subsidiary	
5	Address for Official Communication in India	
6	Name, Designation & Contact of Authorized Signatory	
7	Direct Telephone / Mobile Number	
8	Official E-mail Address	
9	Official Corporate Website	
10	Permanent Account Number (PAN) in India (Attach Copy)	
11	GSTIN Registration Number in India (Attach Copy)	
12	Name & Designation of Dedicated Indian Technical Liaison	

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

ANNEXURE 2: DECLARATION REGARDING PAST EXPERIENCE & TRACK RECORD

(To be printed on Bidder's Official Letterhead)

To:

The Chief Operating Officer,

Foundation for Quantum Computing Innovation (FQCI),

IISc Campus, Bengaluru – 560012, Karnataka, India.

Ref: Tender Ref No. FQCI/NQM/QPU-CLOUD/2026-27/01

I/We hereby certify that our organization / parent OEM has provided cloud-based QPU access, quantum hardware deployments, and quantum developer software toolchains for a continuous period of _____ years.

Details of three (3) major client engagements within the last three (3) years:

#	Client / Academic Organization Name	Scope of Quantum Cloud Access (Modality & Lots)	Contract Period (From - To)	Value of Contract (USD / INR)	Contact Person (Name, Email & Phone)
1					
2					
3					

Copies of relevant Purchase Orders (prices masked)/Agreements/Client Letters/Certificates or a Self-Declaration/Affidavit are enclosed.

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

ANNEXURE 3: DECLARATION OF CLEAN TRACK RECORD & NON-BLACKLISTING

(To be printed on Bidder's Official Letterhead)

To:

The Chief Operating Officer,

Foundation for Quantum Computing Innovation (FQCI),

IISc Campus, Bengaluru – 560012, Karnataka, India.

Ref: Tender Ref No. FQCI/NQM/QPU-CLOUD/2026-27/01

Sir/Madam,

I/We carefully examined the Terms & Conditions contained in Tender Document FQCI/NQM/QPU-CLOUD/2026-27/01. I/We hereby solemnly declare that our company/firm, its directors, and its parent OEM are not currently debarred, blacklisted, or suspended by any Central/State Government Ministry, PSU, Autonomous Research Institute in India, or any statutory authority abroad.

I/We further certify that there are no pending integrity-related disputes or non-performance litigations against our organization that would impede the delivery of cloud QPU services.

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

ANNEXURE 4: UNCONDITIONAL ACCEPTANCE OF TENDER TERMS

(To be printed on Bidder's Official Letterhead)

To:

The Chief Operating Officer,

Foundation for Quantum Computing Innovation (FQCI),

IISc Campus, Bengaluru – 560012, Karnataka, India.

Ref: Tender Ref No. FQCI/NQM/QPU-CLOUD/2026-27/01

Sir/Madam,

I/We hereby declare that I/we have read and understood all the provisions, clauses, technical specifications, governance terms, SAT protocols, support SLAs, and penalty clauses of Tender Document FQCI/NQM/QPU-CLOUD/2026-27/01.

I/We confirm that all provisions of this tender document are unconditionally acceptable to our company without any reservation. I/We certify that I am an authorized signatory competent to bind the bidder legally.

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

ANNEXURE 5: TECHNICAL COMPLIANCE & DEVIATION STATEMENT

(Bidders must complete the specific technical table for the Lot(s) they are bidding on, plus the General Governance & SLA table).

5A. LOT A: SUPERCONDUCTING HARDWARE

Parameter / RFP Requirement	Minimum RFP Specification	Compliance Status (Yes/No)	Specification Offered	Deviations / Remarks
Physical Qubits	≥ 50			
Single-Qubit Gate Fidelity	$\geq 99.9\%$ (Median)			
Two-Qubit Gate Fidelity	$\geq 99.0\%$ (Median)			
Readout Fidelity	$\geq 97.0\%$ (Median)			
Coherence Time (T_1, T_2)	T1 ≥ 100 μs (Median) T2 ≥ 60 μs (Median)			
System Benchmark	$QV \geq 128$ OR $CLOPS \geq 5{,}000$/ Vendor to declare QV and/or CLOPS			
Error Mitigation	ZNE, Dynamical Decoupling/Support through the platform or integrated toolkits			
Calibration Telemetry	Real-time API drift logs			

5B. LOT B: QUANTUM ANNEALING HARDWARE

Parameter / RFP Requirement	Minimum RFP Specification	Compliance Status (Yes/No)	Specification Offered	Deviations / Remarks
Active Qubits	$\geq 2{,}000$ OR Analog ≥ 200 programmable atomic sites			
Hardware Topology	Minimum graph degree of 15 OR Programmable atom geometries with			

	tunable interaction range			
Problem Formulation	QUBO / Ising support			
Logical Variables	≥ 500 fully connected			
Performance Reporting	Time-to-Solution (TTS), Residual Energy			
SDK Integration	Python SDK, Embedding APIs			

5C. LOT C: NEUTRAL-ATOM & TRAPPED-ION HARDWARE

Parameter / RFP Requirement	Minimum RFP Specification	Compliance Status (Yes/No)	Specification Offered	Deviations / Remarks
Physical Qubits / Atoms	≥ 50 physical qubits			
Connectivity	All-to-all OR dynamically reconfigurable			
Single-Qubit Gate Fidelity	$\geq 99.9\%$ (Median)			
Two-Qubit Gate Fidelity	$\geq 99.5\%$ (Median)			
Readout Fidelity	$\geq 98.5\%$ (Median)			
Analog Simulation Mode	Programmable Hamiltonian simulation			

5D. GENERAL GOVERNANCE, SECURITY & SLAs (Mandatory for all bidders)

Parameter / RFP Requirement	Minimum RFP Specification	Compliance Status (Yes/No)	Specification Offered	Deviations / Remarks
Administrative Portal	≥ 20 Admin users, MFA, RBAC			
Tenant Isolation	Across Research Groups (Geographically)			

Automated Alerts	50%, 80%, 100% quota warnings			
SDK Compatibility	Qiskit, PennyLane, Cirq, CUDA-Q, OpenQASM 3			
Platform / API SLA	99.5% Monthly Uptime/ Vendor publishes scheduled availability 7 days ahead			
Physical QPU SLA	90.0% Monthly Uptime/ Vendor publishes scheduled availability 7 days ahead			
Support Resolution	P1 $<$ 4h, P2 $<$ 12h, P3 $<$ 2d			
Compensation Multiplier	1.5x Service Credit for Outages/**automatically be converted** to credits for future QPU, simulator, or classical compute			

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

ANNEXURE 6: NON-DISCLOSURE & INTELLECTUAL PROPERTY UNDERTAKING

(To be printed on Non-Judicial Stamp Paper of Rs. 500/-)

UNDERTAKING FOR ABSOLUTE INTELLECTUAL PROPERTY PROTECTION AND CONFIDENTIALITY

Tender Ref No. FQCI/NQM/QPU-CLOUD/2026-27/01

1. **Undertaking of Exclusivity:** The Bidder/OEM hereby explicitly affirms that all quantum circuits, gate pulses, Hamiltonian matrices, optimization topologies, algorithms, compilation outputs, execution logs, and measurement data submitted or generated by FQCI, NQM researchers, or partner institutions remain the **exclusive, irrevocable intellectual property of FQCI and the originating Indian researchers**.
2. **Non-Usage in Model Training:** The Bidder covenants that neither it nor its technology partners, subcontractors, or backend cloud infrastructure operators shall inspect, analyze, cache, retain, or process FQCI job circuits to train, fine-tune, or benchmark any classical foundation models, predictive algorithms, or commercial optimization engines.
3. **Data Localization & Retention:** All job metadata and user credentials stored within the administrative boundary shall comply with Indian data protection norms. At the expiry of the contract, all tenant environments and execution records shall be securely scrubbed and permanently purged.

Signature of Authorized Representative: _____

Name & Title: _____

Corporate Seal: _____

ANNEXURE 7: STRICT ACCEPTANCE TESTING (SAT) COMPLIANCE UNDERTAKING

(To be printed on Bidder's Official Letterhead)

To:

The Chief Operating Officer,

Foundation for Quantum Computing Innovation (FQCI),

IISc Campus, Bengaluru – 560012, Karnataka, India.

Ref: Tender Ref No. FQCI/NQM/QPU-CLOUD/2026-27/01

We hereby formally accept that quarterly disbursements, contract extensions, and invoice clearances shall remain strictly conditional upon our cloud QPU platform successfully passing the **Strict Acceptance Testing (SAT)** protocols defined under Section 7.1 of this RFP.

We acknowledge that in the event our platform fails to demonstrate the required physical qubit counts, gate fidelities ($1Q \geq 99.9\%$, $2Q \geq 99.0\%$, Readout $\geq 97.0\%$), coherence times ($T_1/T_2 \geq 100\ \mu s/60\ \mu s$), or uptime availability within fourteen (14) days of notification, FQCI retains the absolute right to withhold payouts, enforce $1.5\times$ penalty credits, or terminate the agreement.

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

ANNEXURE 8: COMMERCIAL BID FORMATS (COVER "B")

(To be submitted strictly in Envelope "B" / Financial Cover in INR)

COMMERCIAL BID SCHEDULE

All rates must be quoted in Indian Rupees (INR), exclusive of applicable GST.

Prices must remain firm for three (3) years. Unused hours roll over automatically.

Rate Card for Lot A: Superconducting Quantum Hardware

Service / Hardware Resource	**Billing Unit**	**Shared Queue Rate (INR)**	**Dedicated Reservation Rate (INR)**
Primary Superconducting QPU (≥ 50 Qubits)	Per Hour		
Secondary Superconducting QPU	Per Hour		
Per-Task Submission Fee	Per Task		
Per-Shot Execution Fee	Per Shot		

Rate Card for Lot B: Quantum Annealing Hardware

Service / Hardware Resource	**Billing Unit**	**Shared Queue Rate (INR)**	**Dedicated Reservation Rate (INR)**
Quantum Annealer Access (≥ 2,000 Qubits/ OR Analog ≥ 200 programmable atomic sites)	Per Hour		
Per-Task Submission Fee	Per Task		
Per-Shot Execution Fee	Per Shot		

Rate Card for Lot C: Neutral-Atom & Trapped-Ion Hardware

Service / Hardware Resource	**Billing Unit**	**Shared Queue Rate (INR)**	**Dedicated Reservation Rate (INR)**
Trapped-Ion QPU Access	Per Hour		
Neutral-Atom QPU (Gate-Based Mode)	Per Hour		
Analog Quantum Simulator Mode	Per Hour		
Per-Task Submission Fee	Per Task		

Per-Shot Execution Fee	Per Shot		

Authorized Signatory: _____

Name & Designation: _____

Date & Official Seal: _____

TENDER SUBMISSION CHECKLIST

(To be enclosed within Technical Cover "A")

Sl. No.	***Document Description***	***Enclosed? (Yes / No)***	***Page Reference***
1	*Covering Letter*		
2	***Annexure 1:*** *Bidder Profile & Corporate Details*		
3	*Certificate of Incorporation & Indian Office Registration*		
4	*PAN & Valid GSTIN Clearance Certificates*		
5	*Audited Balance Sheets & P&L Statements (FY 23-24, 24-25, 25-26)*		
6	***Annexure 2:*** *Declaration of Experience & Client Proofs / Self-Declaration*		
7	***Annexure 3:*** *Clean Track Record & Non-Blacklisting Declaration*		
8	***Annexure 4:*** *Unconditional Acceptance of Tender Conditions*		
9	***Annexure 5:*** *Technical Compliance and Deviation Statement (5A - 5D)*		
10	***Annexure 6:*** *Stamped NDA & IP Ownership Undertaking*		
11	***Annexure 7:*** *Strict Acceptance Testing (SAT) Compliance Form*		
12	*OEM Authorization Form (if bid submitted by Indian subsidiary/partner)*		
13	***List of Top 5 to 10 Peer-Reviewed Scientific Publications*** *(Ref. Section 4.8)*		
14	*Signed & Stamped copy of entire RFP document (all pages)*		
15	*Enclosed Envelope "B" (****Annexure 8:*** *Commercial Bid in separate sealed cover)*		